ACS APPLIED MATERIALS & INTERFACES

Research Article

www.acsami.org

Organic Transistor Memory with a Charge Storage Molecular Double-Floating-Gate Monolayer

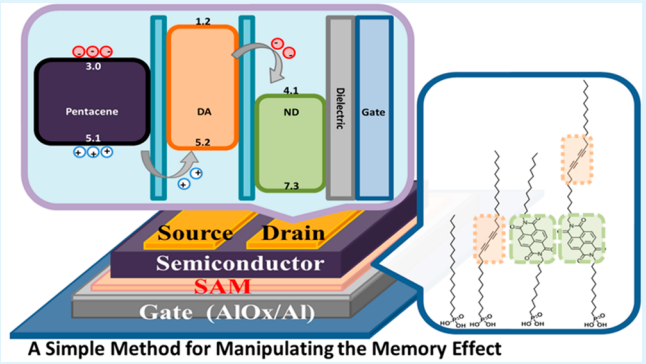
Chiao-Wei Tseng,*[,†] Ding-Chi Huang,[‡] and Yu-Tai Tao*[,†,‡]

[†]Institute of Chemistry, Academia Sinica, Taipei, Taiwan 11529

[‡]Department of Chemistry, National Tsing-Hua University, Hsin-chu, Taiwan 30013

Supporting Information

ABSTRACT: A flexible, low-voltage, and nonvolatile memory device was fabricated by implanting a functional monolayer on an aluminum oxide dielectric surface in a pentacene-based organic transistor. The monolayer-forming molecule contains a phosphonic acid group as the anchoring moiety and a charge-trapping core group flanked between two alkyl chain spacers as the charge trapping site. The memory characteristics strongly depend on the monolayer used due to the localized charge-trapping capability for different core groups, including the diacetylenic (DA) unit as the hole carrier trap, the naphthalenetetracarboxyldiimide (ND) unit as the electron carrier trap, and the one with both DA and ND units present, respectively. The device with the monolayer carrying both DA and ND groups has a larger memory window than that for the one containing DA only and a longer retention time than that for the one containing DA or ND only, giving a memory window of 1.4 V and a retention time around 10^9 s. This device with hybrid organic monolayer/inorganic dielectrics also exhibited rather stable device characteristics upon bending of the polymeric substrate.



A Simple Method for Manipulating the Memory Effect

KEYWORDS: *organic transistor memory devices, flexible field-effect transistors, double-floating gate, self-assembled monolayer, molecular charge traps*

1. INTRODUCTION

To meet the future trend as well as the need for smart, wearable, and foldable devices, organic-based electronics, such as display,[1−3] solar cell,[4−6] radio frequency identification tags (RFID),[7−9] sensors,[10−13] and so on, have attracted much attention in recent years. A memory device is an essential component in many of these electronic devices for data processing, storage, and communication. In a memory device, a material with bistable states either in conductivity,[14−16] magnetism,[17,18] polarization,[19,20] or phase transition[21,22] upon an external stimulus is used to achieve the switching action in computer binary digits. A transistor-type memory is attractive because of a single transistor realization and the compatibility with complementary metal oxide semiconductor devices. The memory effect can be achieved by inserting a charge-trapping floating gate between the semiconductor channel layer and the gate dielectric. The presence or the absence of trapped charges in the floating gate upon the action of gate bias creates a different electrical field to shield the applied gate field and alters the carrier density that can be generated in the channel so that the electric bistability can be installed. Instead of using traditional inorganic materials, organic polymers,[23−27] metallic nanoparticles,[28−32] and organic molecules[33−36] have been demonstrated to act as charge traps, which can induce memory effect in transistor devices.

Self-assembled monolayer (SAM), which is a single molecular layer formed spontaneously on a substrate surface through specific binding interaction, has gained much attention due to the simple fabrication process, the well-defined structural characteristics, and the potential applications in molecule-based electronics.[37,38] Compared to traditional floating gates, the molecular floating gate formed by a SAM has many attractions, including the following: (1) improvement of the device reliability and prevention of charge leakage from the floating gate due to the independent and discrete traps; (2) increase of the density of trapped charges and ability of scaling down the devices for subnanometer-sized device application, because all traps are of molecular dimension; (3) tailorability of device property and function by molecular structure engineering and chemical synthesis; (4) simplified fabrication processes and reduced manufacturing cost (low-cost and low-temperature processing); and (5) suitable applications on flexible substrates.

In this paper, we report a simple method for manipulating the memory effect in a pentacene-based transistor by implanting a SAM, which is composed of a phosphonic acid anchoring group and a charge-storing core group flanked

Received: February 20, 2015
Accepted: April 15, 2015
Published: April 15, 2015

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767−9775

between two alkyl chain spacers, at the interface between the semiconductor channel and the dielectric layer. For low-power application, aluminum oxide, formed directly by plasma-oxidization of an aluminum gate electrode, was used as the dielectric for its high dielectric constant and excellent thermal stability. The memory characteristics can be tuned by varying the structure of the charge-storing core groups, which include the diacetylenic (DA) unit as the hole carrier trap, the naphthalenetetracarboxyldiimide (ND) unit as the electron carrier trap, or both in the monolayer-forming molecule. In comparison, the device with a monolayer containing both DA and ND groups exhibited extended memory retention time and reliable memory characteristics than that for the device containing either group alone. This hybrid organic monolayer/inorganic dielectric device also showed rather stable property upon bending of the flexible substrate. A slight change of device performance depending on the bending direction indicates the relationship between bending strain and carrier mobility. These results demonstrated the great potential application of organic molecular monolayers in flexible nonvolatile memory devices.

2. EXPERIMENTAL SECTION

The structures of phosphonic acids (PA) carrying a DA unit, an ND unit, or both are shown in Figure 1, with the numbers preceding or in

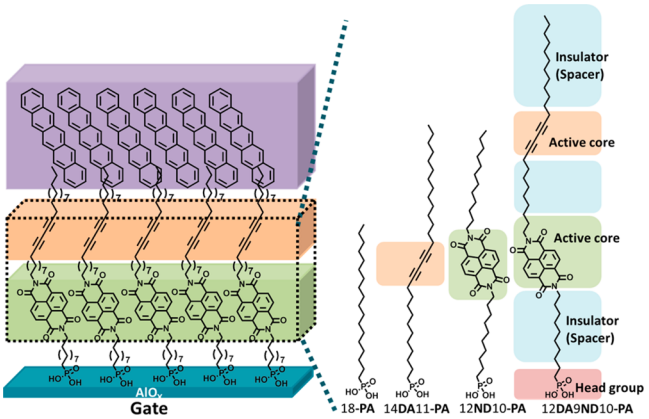


Figure 1. Schematic diagram of the semiconductor/dielectric interface, and the structures and abbreviations of monolayer-forming phosphonic acids used in this study.

between the functional groups in the abbreviations indicating the chain lengths of the alkyl spacer groups. These were synthesized in the laboratory and fully characterized by ^{1}H NMR and ^{13}C NMR and mass spectrometry, respectively (see the Supporting Information).

N-Doped silicon substrates with 300-nm-thick, thermally grown oxide were cleaned by Piranha (70%H_2SO_4:30%H_2O_2) solution, followed by a thorough rinse with pure water and drying with a nitrogen flow. The 200-μm-thick polyethylene terephthalate (PET) substrates were cleaned by sonication in detergent solution, DI water, and acetone in sequence and then dried by a nitrogen flow. A patterned aluminum (30 nm) layer deposited by thermal evaporation through a shadow mask onto the silica and PET substrates, respectively, was used as the gate electrode. An aluminum oxide layer (about 3.8 nm) was formed on the surface of aluminum via oxygen plasma treatment (100 W for 10 min).[39] Monolayers of various phosphonic acids were prepared immediately following oxygen plasma treatment of the aluminum surface by immersing the substrates in 0.1 mM solutions of respective acids for 24 h under ambient conditions, followed by a thorough rinse with pure solvent. For the reference *n*-octadecylphosphonic acid (C18PA) and the DA-carrying PA, tetrahydrofuran (THF) was used as the solvent. For ND- and DA-ND-carrying PA, dimethylformamide (DMF) was used as the solvent. The transistor devices were prepared by depositing 60 nm pentacene film as the channel layer on the SAM-modified substrate at a rate of 0.2 Å/s under a vacuum of 2×10^{-5} Torr. Source and drain electrodes were deposited through a shadow mask with a channel length of 50 μm and a channel width of 500 μm to complete the top-contact, bottom-gate FET device.

Reflection absorption infrared spectra (RAIRS) of the adsorbed monolayers on aluminum oxide surfaces were recorded with a Varian 640-IR spectrometer equipped with a MCT detector at 4 cm^{-1} resolution at room temperature. The thickness of the monolayer was measured by an ellipsometer. Contact angle was measured by the DIGIDROP GBX contact angle meter using ultrapure water as the wetting liquid. The powder X-ray diffraction measurements were carried out with a Philips X'Pert diffractometer equipped with an X'Celerator detector. Atomic force microscopy analyses were carried out with a Multimode Atomic Force Microscope (Digital Instruments, Nanoscope III) using tapping mode with a silicon tip. The capacitances of the hybrid SAM/AlO_x dielectric were measured by impedance spectroscopy (the Solartron 1260 Impedance/Gain-Phase analyzer) for frequencies between 100 Hz and 100 kHz. The electrical characteristics of the transistor devices were measured in ambient at room temperature with a HP4156 Parameter Analyzer.

3. RESULTS AND DISCUSSION

3.1. Characterization of the surface films. The adsorption of phosphonic acid on an aluminum oxide surface takes place via surface anchoring and condensation reaction between the phosphonic acid group and the surface hydroxyl group.[40] Water contact angle measurement was used to roughly monitor the monolayer formation process. Prior to the self-assembly, the plasma-treated aluminum has a contact angle below 5°. The contact angle quickly increased with increasing immersing time of the substrate in the phosphonic acid solutions initially, and then reached nearly a constant value. After self-assembly of the monolayers, hydrophobic character ($\theta(H_2O) > 90°$) was obtained in all cases (Figure 2b). Ellipsometry and the RAIRS were used to confirm the presence of a monolayer (Figure 2a and 2b). The two methylene stretching modes, asymmetric and symmetric stretching, present in the RAIRS spectra of the SAMs are at around 2918 and 2850 cm^{-1} for the reference monolayer and the DA-containing monolayer, which is indicative of *trans*-zigzag conformation and solid state of the hydrocarbon chains. For ND- and DA-ND-containing monolayers, slight shifts to higher frequencies of 2925 and 2854 cm^{-1} indicate more disordering of the packing. Together with ellipsometry data, a closely packed monolayer is suggested with all the compounds used. The leakage current density versus bias voltage through the monolayer and the frequency-dependent capacitances for the hybrid dielectric of the SAM/AlO_x film were measured using a metal−insulator−metal (MIM) structure with gold top electrodes and aluminum bottom electrodes (Au/SAM/AlO_x/Al). The results are shown in Figure 2c and 2d. The low leakage current density (10^{-6} A at −3 V) and nearly frequency-independent capacitances indicate a good dielectric property of the hybrid dielectric layer prepared. Pentacene films deposited on the monolayer-covered AlO_x surface were characterized by X-ray diffraction, which shows typical diffraction peaks for pentacene films at 2θ = 5.8° (001) and 11.5° (002), respectively. AFM microscopy shows the morphology of these films to be layered polycrystalline grains (Figure 3). A small dependence of the diffraction peak intensity and grain size of the pentacene films on differently modified substrates was

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767−9775

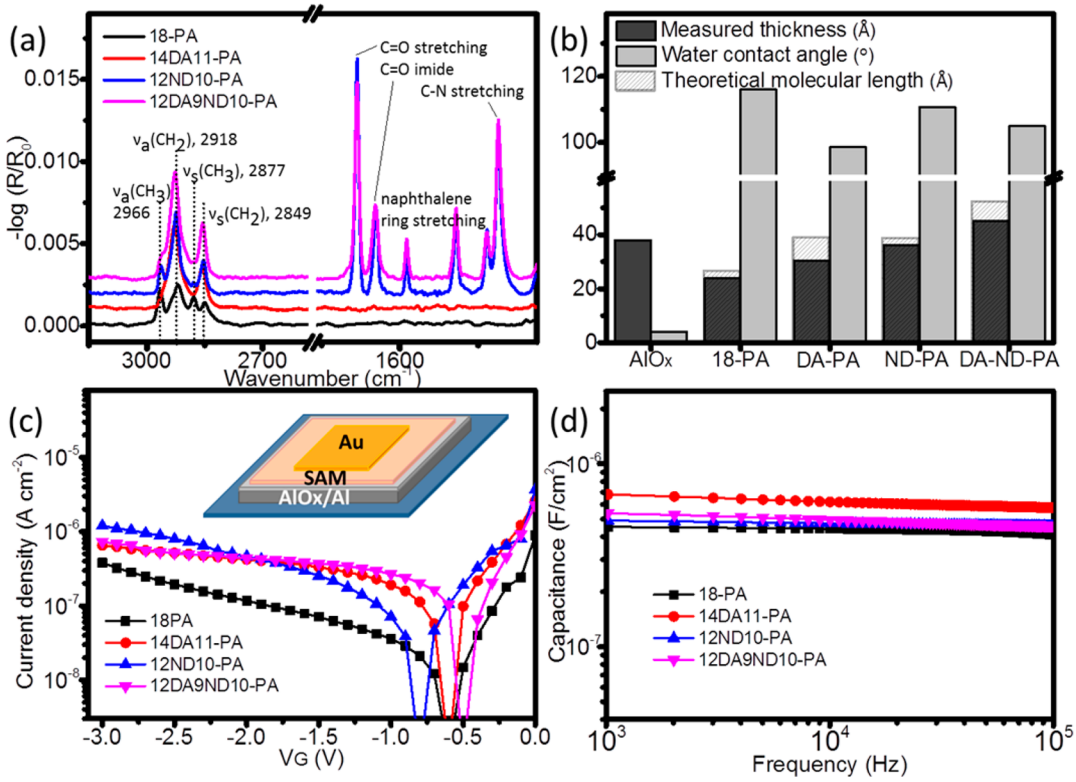


Figure 2. (a) Reflection–absorption IR spectra of various monolayers on plasma-oxidized aluminum (AlO_x). (b) Monolayer thickness measured by the ellipsometry and by Spartan simulation, and the water contact angle of SAM-modified AlO_x surfaces. (c) Leakage current density and (d) capacitances of different hybrid SAMs/AlO_x gate dielectrics. Inset: Schematic diagram showing the metal–insulator–metal (Au/SAMs/AlO_x/Al) capacitor structure used for characterizing the leakage current density and capacitance of the hybrid dielectrics.

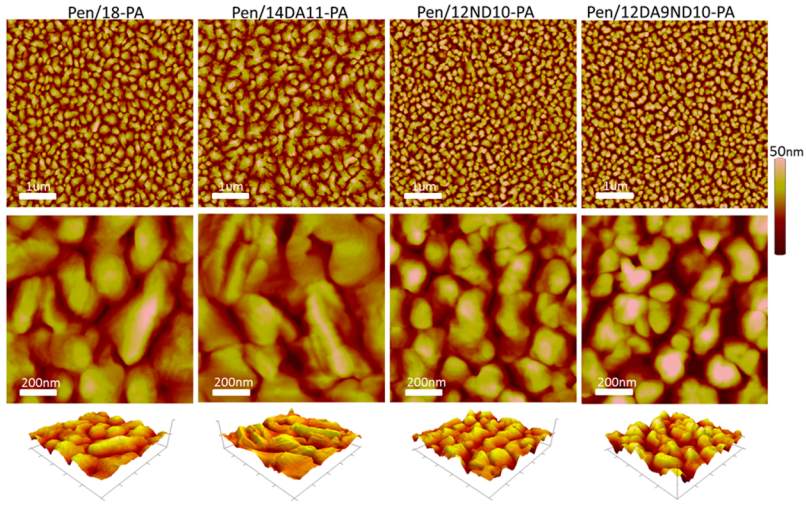


Figure 3. AFM images of pentacene films deposited on various phosphonic acid monolayer-modified aluminum oxide substrates.

observed, which might be due to the surface roughness from molecular domain boundaries and defects in the monolayers.[41,42]

3.2. Electric properties. The output characteristics of the functional SAM-based transistors are shown in the Supporting Information (Figure S1). The transfer characteristics of the transistors show typical p-type behavior in that increasing currents were obtained with increasingly negative gate bias as the gate bias was swept from positive value (+1 V) to negative value (−3 V) (Figure 4). Field-effect mobility data and other device parameters extracted from the *I*–*V* characteristics are listed in Table 1. The reference devices with the aliphatic (*n*-octadecylphosphonic acid) monolayer exhibited a charge mobility of 0.16 cm^2/(V s) and an on/off current ratio of 10^5, which are typical values for pentacene-based transistors with SAM/AlO_x dielectrics.[43,44] The threshold voltage shifted to more positive values for devices with ND-carrying monolayer incorporated at the surface, compared to that of the reference device, whereas with DA-carrying monolayer incorporated, the threshold voltage shifted to more negative values (Table 1). With both ND and DA groups present, the threshold voltage is similar to that of the reference device. The

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767–9775

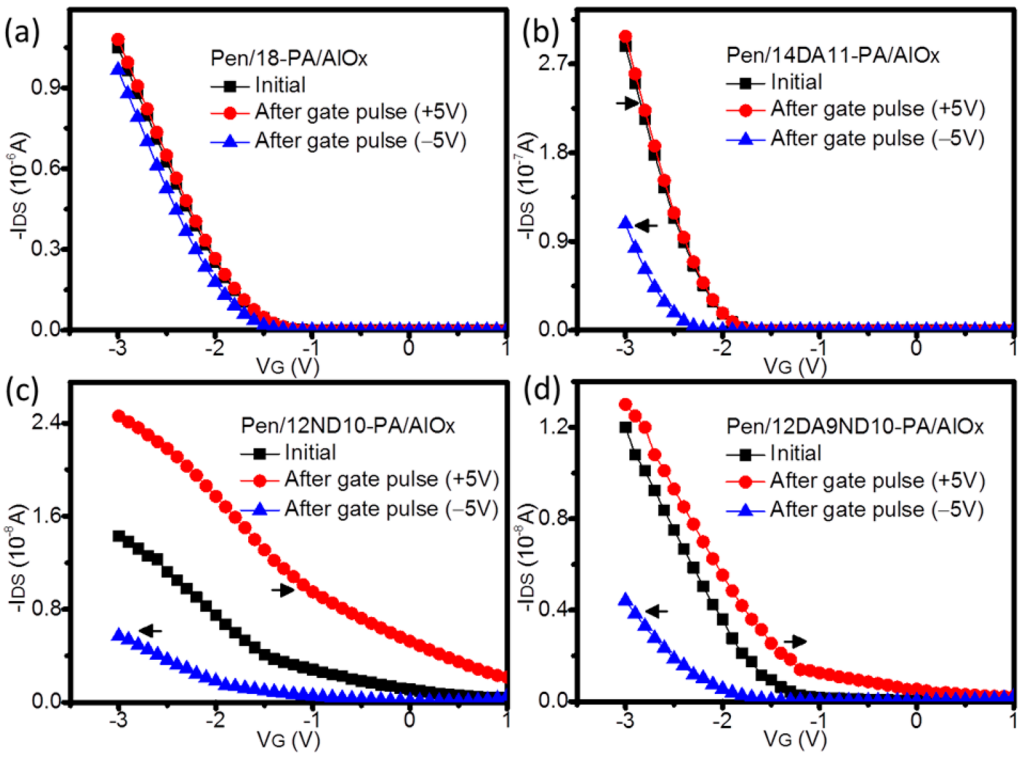


Figure 4. Transfer characteristics of the devices with the monolayer of (a) 18-PA, (b) 14DA11-PA, (c) 12ND10-PA, and (d) 12DA9ND10-PA after a gate bias pulse of +5 V/−5 V for 18 s, respectively.

Table 1. Device Characteristics as a Function of Surface Modification of Aluminum Oxide Dielectrics

Pen/SAM/Al_2O_3	Threshold Voltage [V]	Capacitance [nF/cm^2][a]	Mobility [cm^2/(V s)]	On−Off ratio	Memory Window [V]	Stored Charges/cm^2	Charges/ Molecule	Retention [s][b]
18-PA	−1.1	452	0.16	10^5	0.1			
14DA11-PA	−1.7	680	6.3×10^{-2}	10^3	0.5	2.1×10^{12}	6.0×10^{-3}	10^5
12ND10-PA	0.4	490	6.1×10^{-4}	10^2	3.3	1.0×10^{13}	2.8×10^{-2}	10^4
12DA9ND10-PA	−1.0	537	2.4×10^{-3}	10^3	1.4	4.8×10^{12}	1.3×10^{-2}	10^9

[a]The field-effect mobility was calculated using the expression that describes the drain current at the saturation regime. [b]Estimated by extrapolating the ON and OFF currents.

opposite behavior is presumably due to different carrier-storing ability: the strong electron-accepting ND moiety can better stabilize electron carriers so that hole carriers are induced or generated at less negative bias and the threshold voltage shifts in a more positive direction, while the DA unit can stabilize positive charge and thus can trap the hole carriers and more negative bias is needed to generate free hole carriers in the channel, leading to more negative threshold voltage.[45,46] The transistors were also biased with positive and negative gate pulses to explore the nature of charging behavior for the potential of memory applications. The transfer characteristics at the initial state, programmed state (−5 V for 18s), and erased state (+5 V for 18s) are also included in Figure 4. For the control transistor with merely alkyl monolayer incorporated, transfer curve shift was negligible (about 0.1 V) after different gate bias pulses. However, with DA-containing monolayer at the dielectric surface, a positive prepulse did not cause any shift in the threshold voltage V_{th}. A negative prepulse caused significant V_{th} shift (0.6 V) in the negative direction. This could mean a positive prepulse did not generate electron carriers at the interface, or the electron carriers generated at the interface could not be stabilized and trapped by the DA-containing monolayer. A negative prepulse generated hole carriers, which can be trapped and stabilized by the DA moieties and influenced the V_{th}. In contrast, with an ND-containing monolayer, a positive prepulse caused significant V_{th} shift in the positive direction and a negative prepulse also shifted the V_{th} to the negative direction. This could mean that both charge carriers, positive or negative, generated upon the gate pulse can be trapped by the ND units in the monolayer. That ND can trap hole carriers is more or less unexpected, even though holes and electrons were reported to be trapped in the electron-accepting molecules such as C60 when they were embedded into a pentacene-based transistor.[33] Nevertheless, as can be seen later, the ND system cannot seem to stabilize the hole carriers well enough so that the positive charges are lost fast. In the system with both DA and ND moieties incorporated, the V_{th} can shift in either direction, depending on the original pulse, presumably for the same reasons cited above. The extent of positive shift was smaller than that containing ND alone, presumably because the ND moiety in this system is located farther away from the pentacene/dielectric interface by an additional alkyl chain and the DA unit so that electron carrier trapping is less efficient. It is worth noting that when two

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767−9775

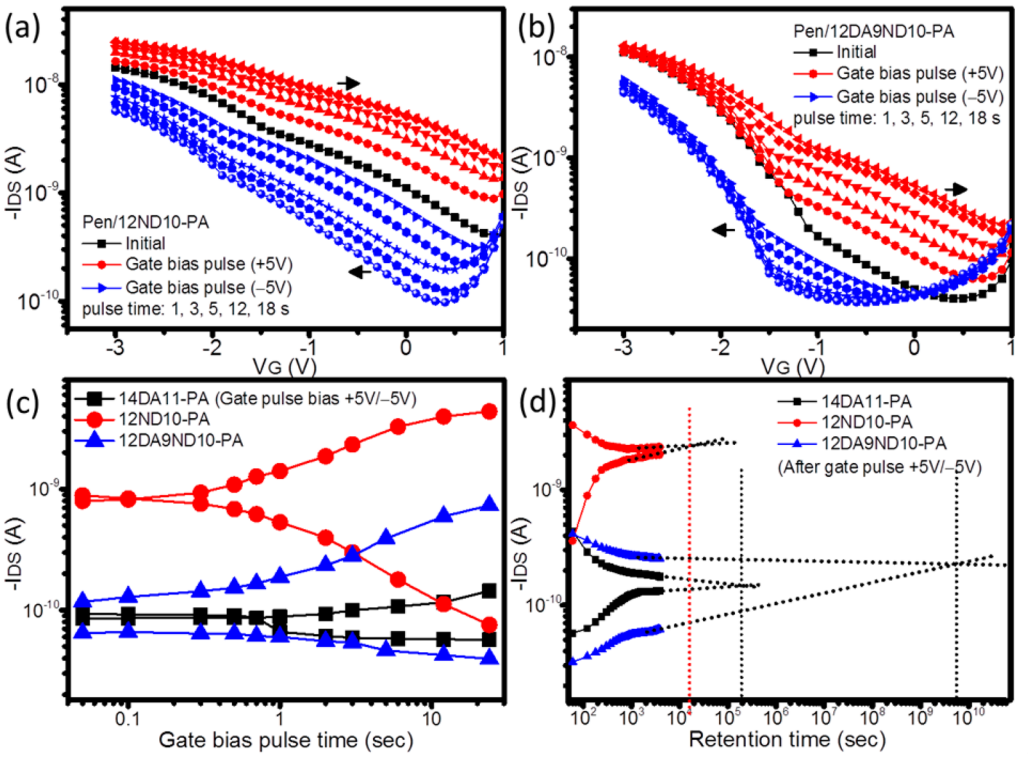


Figure 5. (a–b) Transfer characteristics of devices with a monolayer of 12ND10-PA and 12DA9ND10-PA as a function of +5 V/-5 V gate bias for different pulse durations, respectively. (c) Drain current as a function of gate bias pulse time for the devices with 14DA11-PA, 12ND10-PA and 12DA9ND10-PA SAMs, respectively. (d) Retention characteristics of the corresponding devices with a SAM of 14DA11-PA, 12ND10-PA and 12DA9ND10-PA, respectively.

charge trapping moieties are present with different distances from the semiconductor layer, the transfer curve shift behavior is unusual. As shown in Figure 5, the transfer curve normally shifts steadily with increasing prepulse time and presumably more and more charges are stored with longer pulse time. Nevertheless, with DA-ND-containing monolayer, a negative prepulse of different duration yielded rather small shifts in the transfer curves. It is suggested that the prepulse charges up the DA unit quickly, which blocks the further charging of the ND unit underneath. This will lead to small changes in the hole charges with pulse time. A positive prepulse cannot charge up the DA unit. Rather it will charge up the ND unit gradually because the ND unit is buried down under. The transfer curves show different sensitivity to the pulse time at the low bias (OFF) state and high bias (ON) state, presumably because the electron charges trapped in the ND unit are low because of the distance. The current change is more sensitive with the gate bias pulse in the OFF state than the ON state. On the other hand, when a negative pulse (programming) was followed by a positive pulse (erasing), the shifted transfer curve restored to nearly its original position in the DA-containing device, whereas further shift in the positive direction was observed for the ND-containing and DA-ND-containing devices. These results suggest that, besides detrapping the holes, electron-trapping occurred as well in the systems containing ND- and DA-ND-monolayers when a positive gate bias was applied. The shifts in the transfer curves between the programmed and erased states were repeatable. The resulting V_{th} shifts, referred to as the memory window, are summarized in Table 1.

Relating the switching responses to the programming/erasing action, the source-drain current changes as a function of initial gate pulse time are shown in Figure 5c. Upon positive gate bias (+5 V), currents for the DA-ND-containing device and in particular the ND-containing device reached their maximum values (ON state) quickly, whereas for the DA-containing device, the "ON" current increased marginally and remained nearly constant for pulse times smaller than 10 s. Upon negative gate bias (−5 V), the DA-ND-containing device and especially the DA-containing device reached their minimum current (OFF state) rapidly, in about 5 s for the DA-containing device and around 10 s for the DA-ND-containing device, whereas the ND-containing system did not yet reach its minimum even after 24 s. These results suggest that the DA-ND-containing system was able to reach both maximum and minimum currents fast. Similar results could also be seen in the shifts of transfer curve as a function of gate pulse time in Figure 5a and 5b. Thus, this system is most responsive to the programing/erasing action. Moreover, the currents obtained as a function of time elapsed after the gate bias pulse (−5 V/+5 V) was turned off are shown in Figure 5d, which relates to the retention properties. The OFF-state current gradually increased in the DA- and DA-ND-containing devices, but the ND-containing device showed a much mroe rapid current increase. On the other hand, the "ON" current decayed much quicker in the DA-containing system than in the ND-containing and the DA-ND-containing systems. The DA-ND-containing system has a much longer retention time than the other two systems. These results can be rationalized as follows. With the gate bias applied, charge carriers are induced and accumulated at the semiconductor/monolayer interface. Some of the carriers will transfer to the core moieties and be trapped there. By applying a reverse bias at the gate, the trapped charges

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767–9775

will be dispelled (discharged) from the core moieties. The efficiency for the molecular layers to be charged and discharged depends on the separating alkyl chain length and the Schottky barrier existing between the semiconductor and the core moieties.[16,47] As similar alkyl chain length is used to separate DA or ND from the pentacene layer, thus the Schottky barrier is the determining factor. As shown in the energy level alignment diagram in Figure 6, the HOMO level of DA is close

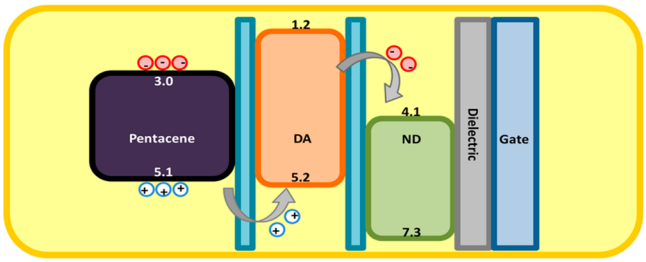


Figure 6. Energy-band diagram in zero-gate-voltage configuration of the transistor with SAMs.

to the HOMO level of pentacene. With a negative gate pulse, the hole carriers induced in the pentacene layer can transfer to the DA moieties, after overcoming the insulating alkyl chain barrier. These trapped positive charges partly offset the gate bias and shift the transfer curve in the negative direction, resulting in a lower "OFF" current. As the energy levels are closer, the charge transfer occurs relatively quickly and thus the minimum "OFF" current is reached rapidly. In contrast, a higher Schottky barrier hinders the transfer of electron carriers to the DA moieties, so that the shift in transfer curve is small and the "ON" current increases only slowly. In the ND-containing system, a low LUMO level makes the electrons transfer to ND easier, and the transfer back to pentacene harder, due to the Schottky barrier formed. Thus, the maximum ON-current is achieved quickly and this ON-state current decays only slowly with time. On the other hand, a low HOMO level of ND makes the holes transfer to the ND moieties less facilely and the trapped positive charges, if any, return back to pentacene layer easily, so that the minimum OFF-current is reached more slowly and its OFF-state current quickly increases with time once the bias is removed. However, in the monolayer containing both DA and ND moieties, not only can the hole charges transfer to the DA moieties readily and be trapped there, but electron charges can also be trapped and stored by ND moieties, although the trapping of electron carrier becomes more sluggish due to the DA moiety and the additional alkyl

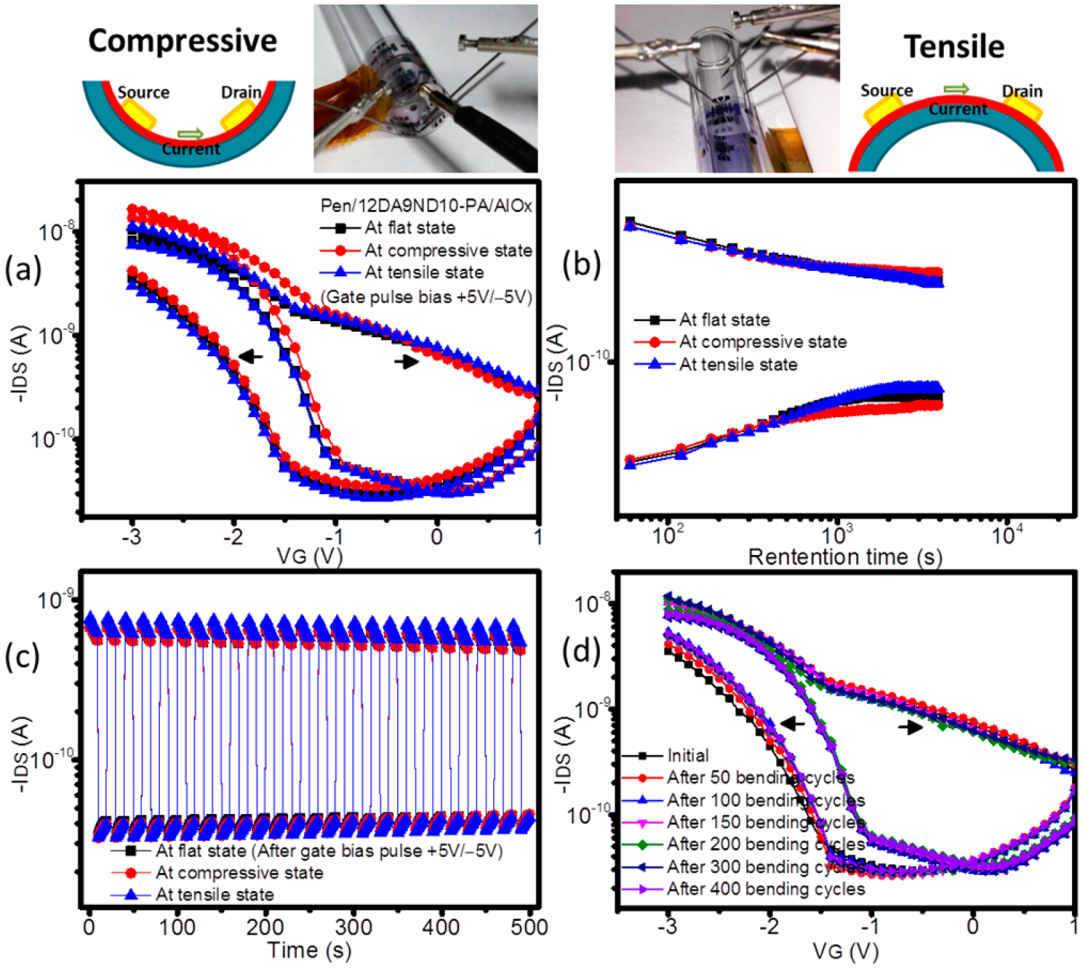


Figure 7. (a) Transfer characteristics of the 12DA9ND10-PA device at the flat state, compressive state and tensile state after gate bias pulse of +5 V/-5 V, respectively. (b) Drain current retention characteristics of the corresponding device at the flat state, compressive state and tensile state, after gate bias pulse of +5 V/-5 V, respectively. (c) Reversible switching between ON-state and OFF-state of the corresponding device at the flat state, compressive state and tensile state, respectively. (d) Transfer characteristics as a function of bending cycles.

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767–9775

spacer imposed between ND and pentacene. A large memory window, fast response time, and much longer charge retention time can be observed. When comparing with a DA-containing system, the DA-ND system exhibits a much larger transfer curve shift due to the contribution of trapped electron carriers by the ND moieties. When comparing with an ND system, the DA-ND system shows longer charge retention time because of trapping and stabilization of hole carriers (leading to the OFF-current) by the DA moieties.

The number of trapped charges in the monolayer can be estimated according to eq 1.[48]

$$\Delta V_{th} = \frac{d_i Q}{\varepsilon_i} = -\frac{Q}{C_i} \quad (1)$$

where ΔV_{th} is the threshold voltage shift and C_i is the dielectric capacitance. For a DA-ND-containing system, the density of trapped charges is calculated to be 4.8×10^{12} cm^{-2}, based on its maximum threshold voltage shift of 1.4 V and the dielectric capacitance of 5.37×10^{-7} F cm^{-2} for the dielectric layer of the DA-ND monolayer/aluminum oxide composite. The density of molecules in the molecular monolayer is 3.69×10^{14} cm^{-2}, estimated from the molecular cross-section area of 27.1 Å^2 in a closely packed monolayer. About one charge per 100 molecules is estimated. The trapped charge density in other systems is summarized in Table 1.

3.3. Effect of substrate bending. For potential application in flexible electronics, a stable performance upon substrate bending is necessary. Bending may introduce stress at the interfaces, resulting in changes in the packing and intermolecular distances, which may change the electronic coupling between neighboring molecules.[49,50] The memory effect upon mechanical bending of a DA-ND-containing device was also tested. The pentacene-based transistor with the hybrid dielectric layer of a DA-ND monolayer/AlO_x fabricated on a PET substrate was bent along the axis perpendicular to the direction of charge transport and into a curved surface with a radius of 12.5 mm. The compressive face and the tensile face refer to the concave and convex sides of the bent substrate, respectively, as illustrated in Figure 7.

The DA-ND-containing device showed changes of transfer curves depending on the bending direction. Comparing with a flat state, the current increased at the compressive face (by ~46%) and decreased slightly at the tensile state (by ~8%) (Figure 7a). These current changes were reversible and repeatable when the substrate was bent or flattened. Similar current changes upon bending have been observed previously.[49,51] For the pentacene thin film transistor, charge transport is typically suggested to involve successive hopping between pentacene molecules.[52,53] In the compressive face, the spacing between molecules is expected to decrease and the electronic coupling is expected to increase, which can lead to a larger electronic coupling and thus more efficient charge transport (increasing the current), as illustrated in Figure 8. In contrast, larger hopping distance due to increasing spacing results in lower electronic coupling and thus slowing down the charge transport (decreasing the current), under tensile strain. Alternatively, the changes may just be due to the changes in the distances between the grains in the polycrystalline pentacene film. After the same gate bias pulse, the transfer curve shift (memory window) is slightly larger at tensile state (1.5 V) than that at others (1.2 V at compressive state and 1.3 V at initial state) (Figure 7a). When comparing the charge retention time,

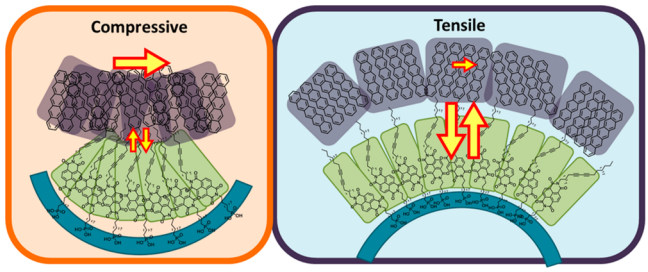


Figure 8. Schematic illustrations of the charge transport and the charge trapping/detrapping processes at the compressive state and the tensile state.

a quick ON-current decay and a rapid OFF-current increase were observed at tensile state (the retention time estimated by extrapolating the ON and OFF currents is about 10^7 s) (Figure 7b). However, a smaller transfer curve shift (1.2 V) and a longer charge retention time (about 10^{11} s) could be obtained at compressive state. These can be attributed to the "effective" thickness of the insulating dielectric (molecular alkyl chain) changes under the bending strain.[50] The effective thickness increases due to the smaller spacing between alkyl chains (that is, more hydrocarbon chains per unit volume) under compressive strain, so that it is more difficult for charges to be trapped into the storage sites. This will lead to a smaller transfer curve shift. For the same reason, the trapped charges have lower tendency to leave the trapping sites and thus a longer retention time is obtained, as illustrated in Figure 8. On the other hand, under tensile strain, increasing the spacing between alkyl chains reduces the effective insulator thickness and facilitates trapping of charge carriers at the interface (larger threshold voltage shift) and facilitates detrapping of trapped charges as well (reduced retention time).

The repetitive switching of the memory device via the write-read-erase-read cycles (WRER) at the flat, compressive, and tensile states is shown in Figure 7c. The writing and erasing was carried out by applying a gate bias of −5 V/+5 V for 10 and 18 s, respectively, and the reading was carried out by measuring the drain current without any gate bias applied. The bending radius was 12.5 mm at both compressive and tensile states. Well-separated ON and OFF currents could be maintained over repeated cycles. The stability of the memory transistor upon bending was demonstrated by recording the initial transfer curve and programmed/erased transfer curves with respect to the bending cycles, as shown in Figure 7d. One bending cycle refers to bending the substrate at both compressive and tensile states. The performance of transistor memory could be well maintained over 400 bending cycles. The reliability and reversibility of the current switching and transfer curves suggest the system has a potential for application in flexible electronics.

4. CONCLUSION

Low-voltage, electric bistability of a pentacene-based transistor can be achieved by simply inserting a self-assembled monolayer of charge-storing molecules on a plasma-oxidized aluminum gate surface. The device performance can be further modulated by tailoring the molecular structure of the monolayer. The device with a molecule containing trapping sites for both electrons and holes at the same time exhibited a long data retention time and reliable memory characteristics. This hybrid organic SAM/inorganic dielectric device which showed good

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767−9775

mechanical stability upon bending of the flexible substrates offers a great potential for applications in future smart wearable electronics.

■ ASSOCIATED CONTENT

Supporting Information

Syntheses and characterization of various phosphonic acids. This material is available free of charge via the Internet at http://pubs.acs.org.

■ AUTHOR INFORMATION

Corresponding Authors

*E-mail: alextseng@gate.sinica.edu.tw.
*E-mail: ytt@gate.sinica.edu.tw.

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

This work was supported by the Ministry of Science and Technology, Taiwan, Republic of China through Grant No. 101-2113-M-001-006-MY3.

■ REFERENCES

(1) Hernandez-Sosa, G.; Tekoglu, S.; Stolz, S.; Eckstein, R.; Teusch, C.; Trapp, J.; Lemmer, U.; Hamburger, M.; Mechau, N. The Compromises of Printing Organic Electronics: A Case Study of Gravure-Printed Light-Emitting Electrochemical Cells. *Adv. Mater.* **2014**, *26*, 3235−3240.

(2) Murawski, C.; Leo, K.; Gather, M. C. Efficiency Roll-Off in Organic Light-Emitting Diodes. *Adv. Mater.* **2013**, *25*, 6801−6827.

(3) Sandström, A.; Dam, H. F.; Krebs, F. C.; Edman, L. Ambient Fabrication of Flexible and Large-Area Organic Light-Emitting Devices Using Slot-Die Coating. *Nat. Commun.* **2012**, *3*, 1002−1006.

(4) Li, K.; Zhen, H.; Niu, L.; Fang, X.; Zhang, Y.; Guo, R.; Yu, Y.; Yan, F.; Li, H.; Zheng, Z. Full-Solution Processed Flexible Organic Solar Cells Using Low-Cost Printable Copper Electrodes. *Adv. Mater.* **2014**, *26*, 7271−7278.

(5) Wang, W.; Song, M.; Bae, T. S.; Park, Y. H.; Kang, Y. C.; Lee, S. G.; Kim, S. Y.; Kim, D. H.; Lee, S.; Min, G.; Lee, G. H.; Kang, J. W.; Yun, J. Transparent Ultrathin Oxygen-Doped Silver Electrodes for Flexible Organic Solar Cells. *Adv. Funct. Mater.* **2014**, *24*, 1551−1561.

(6) Xie, K.; Wei, B. Materials and Structures for Stretchable Energy Storage and Conversion Devices. *Adv. Mater.* **2014**, *26*, 3592−3617.

(7) Gelinck, G.; Heremans, P.; Nomoto, K.; Anthopoulos, T. D. Organic Transistors in Optical Displays and Microelectronic Applications. *Adv. Mater.* **2010**, *22*, 3778−3798.

(8) Baeg, K. J.; Caironi, M.; Noh, Y. Y. Toward Printed Integrated Circuits based on Unipolar or Ambipolar Polymer Semiconductors. *Adv. Mater.* **2013**, *25*, 4210−4244.

(9) Zhan, Y.; Mei, Y.; Zheng, L. Materials Capability and Device Performance in Flexible Electronics for the Internet of Things. *J. Mater. Chem. C* **2014**, *2*, 1220−1232.

(10) Sekitani, T.; Yokota, T.; Zschieschang, U.; Klauk, H.; Bauer, S.; Takeuchi, K.; Takamiya, M.; Sakurai, T.; Someya, T. Organic Nonvolatile Memory Transistors for Flexible Sensor Arrays. *Science* **2009**, *326*, 1516−1519.

(11) Knopfmacher, O.; Hammock, M. L.; Appleton, A. L.; Schwartz, G.; Mei, J.; Lei, T.; Pei, J.; Bao, Z. Highly Stable Organic Polymer Field-Effect Transistor Sensor for Selective Detection in The Marine Environment. *Nat. Commun.* **2014**, *5*, 2954−2962.

(12) Kulkarni, G. S.; Reddy, K.; Zhong, Z.; Fan, X. Graphene Nanoelectronic Heterodyne Sensor for Rapid and Sensitive Vapor Detection. *Nat. Commun.* **2014**, *5*, 4376−4382.

(13) Zeng, W.; Shu, L.; Li, Q.; Chen, S.; Wang, F.; Tao, X. M. Fiber-Based Wearable Electronics: A Review of Materials, Fabrication, Devices, and Applications. *Adv. Mater.* **2014**, *26*, 5310−5336.

(14) Sun, H.; Liu, Q.; Li, C.; Long, S.; Lv, H.; Bi, C.; Huo, Z.; Li, L.; Liu, M. Direct Observation of Conversion Between Threshold Switching and Memory Switching Induced by Conductive Filament Morphology. *Adv. Funct. Mater.* **2014**, *24*, 5679−5686.

(15) Lin, W. P.; Liu, S. J.; Gong, T.; Zhao, Q.; Huang, W. Polymer-Based Resistive Memory Materials and Devices. *Adv. Mater.* **2014**, *26*, 570−606.

(16) Tseng, C. W.; Tao, Y. T. Electric Bistability in Pentacene Film-Based Transistor Embedding Gold Nanoparticles. *J. Am. Chem. Soc.* **2009**, *131*, 12441−12450.

(17) Cuellar, F. A.; Liu, Y. H.; Salafranca, J.; Nemes, N.; Iborra, E.; Sanchez-Santolino, G.; Varela, M.; Garcia Hernandez, M.; Freeland, J. W.; Zhernenkov, M.; Fitzsimmons, M. R.; Okamoto, S.; Pennycook, S. J.; Bibes, M.; Barthélémy, A.; te Velthuis, S. G. E.; Sefrioui, Z.; Leon, C.; Santamaria, J. Reversible Electric-Field Control of Magnetization at Oxide Interfaces. *Nat. Commun.* **2014**, *5*, 4215−4222.

(18) Wang, Y.; Song, C.; Wang, G.; Miao, J.; Zeng, F.; Pan, F. Anti-Ferromagnet Controlled Tunneling Magnetoresistance. *Adv. Funct. Mater.* **2014**, *24*, 6806−6810.

(19) Rana, A.; Lu, H.; Bogle, K.; Zhang, Q.; Vasudevan, R.; Thakare, V.; Gruverman, A.; Ogale, S.; Valanoor, N. Scaling Behavior of Resistive Switching in Epitaxial Bismuth Ferrite Heterostructures. *Adv. Funct. Mater.* **2014**, *24*, 3962−3969.

(20) Orgiu, E.; Samorì, P. Organic Electronics Marries Photochromism: Generation of Multifunctional Interfaces, Materials, and Devices. *Adv. Mater.* **2014**, *26*, 1827−1845.

(21) Han, Y.; Yuan, X.; Zhu, M.; Li, S.; Whitcombe, M. J.; Piletsky, S. A. A Catalytic and Shape-Memory Polymer Reactor. *Adv. Funct. Mater.* **2014**, *24*, 4996−5001.

(22) Cui, B.; Song, C.; Wang, G.; Yan, Y.; Peng, J.; Miao, J.; Mao, H.; Li, F.; Chen, C.; Zeng, F.; Pan, F. Reversible Ferromagnetic Phase Transition in Electrode-Gated Manganites. *Adv. Funct. Mater.* **2014**, *24*, 7233−7240.

(23) Chiu, Y. C.; Otsuka, I.; Halila, S.; Borsali, R.; Chen, W. C. High-Performance Nonvolatile Transistor Memories of Pentacence Using the Green Electrets of Sugar-based Block Copolymers and Their Supramolecules. *Adv. Funct. Mater.* **2014**, *24*, 4240−4249.

(24) Chiu, Y. C.; Chen, T. Y.; Chen, Y.; Satoh, T.; Kakuchi, T.; Chen, W. C. High-Performance Nonvolatile Organic Transistor Memory Devices Using the Electrets of Semiconducting Blends. *ACS Appl. Mater. Interfaces* **2014**, *6*, 12780−12788.

(25) Nam, S.; Ko, Y. G.; Hahm, S. G.; Park, S.; Seo, J.; Lee, H.; Kim, H.; Ree, M.; Kim, Y. Organic Nonvolatile Memory Transistors with Self-Doped Polymer Energy Well Structures. *NPG Asia Mater.* **2013**, *5*, e33.

(26) Tseng, C. W.; Tao, Y. T. Organic Field-Effect Transistor/Memory Devices with Pentacene/Polydiacetylene Composite Film as Active Channel Material: A Morphology Dependence Study. *ACS Appl. Mater. Interfaces* **2010**, *2*, 3231−3240.

(27) Shang, L.; Ji, Z.; Wang, H.; Chen, Y.; Liu, X.; Han, M.; Liu, M. Low-Voltage Multilevel Memory Based on Organic Thin-Film Transistor. *IEEE Electron Device Lett.* **2011**, *32*, 1451−1453.

(28) Zhou, Y.; Han, S. T.; Chen, X.; Wang, F.; Tang, Y. B.; Roy, V. A. L. An Upconverted Photonic Nonvolatile Memory. *Nat. Commun.* **2014**, *5*, 4720−4727.

(29) Han, S. T.; Zhou, Y.; Yang, Q. D.; Zhou, L.; Huang, L. B.; Yan, Y.; Lee, C. S.; Roy, V. A. L. Energy-Band Engineering for Tunable Memory Characteristics through Controlled Doping of Reduced Graphene Oxide. *ACS Nano* **2014**, *8*, 1923−1931.

(30) Tseng, C. W.; Huang, D. C.; Tao, Y. T. Azobenzene-Functionalized Gold Nanoparticles as Hybrid Double-Floating-Gate in Pentacene Thin-Film Transistors/Memories with Enhanced Response, Retention, and Memory Windows. *ACS Appl. Mater. Interfaces* **2013**, *5*, 9528−9536.

(31) Kang, M.; Baeg, K. J.; Khim, D.; Noh, Y. Y.; Kim, D. Y. Printed, Flexible, Organic Nano-Floating-Gate Memory: Effects of Metal Nanoparticles and Blocking Dielectrics on Memory Characteristics. *Adv. Funct. Mater.* **2013**, *23*, 3503−3512.

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767−9775

(32) Wang, H.; Ji, Z.; Shang, L.; Chen, Y.; Han, M.; Liu, X.; Peng, Y.; Liu, M. Nonvolatile Nano-Crystal Floating Gate OFET Memory with Light Assisted Program. *Org. Electron.* **2011**, *12*, 1236−1240.
(33) Zhou, Y.; Han, S. T.; Yan, Y.; Huang, L. B.; Zhou, L.; Huang, J.; Roy, V. A. L. Solution Processed Molecular Floating Gate for Flexible Flash Memories. *Sci. Rep.* **2013**, *3*, 3093−3101.
(34) Zhang, L.; Wu, T.; Guo, Y.; Zhao, Y.; Sun, X.; Wen, Y.; Yu, G.; Liu, Y. Large-Area, Flexible Imaging Arrays Constructed by Light-Charge Organic Memories. *Sci. Rep.* **2013**, *3*, 1080−1088.
(35) Tseng, C. W.; Huang, D. C.; Tao, Y. T. Electric Bistability Induced by Incorporating Self-Assembled Monolayers/aggregated Clusters of Azobenzene Derivatives in Pentacene-Based Thin-Film Transistors. *ACS Appl. Mater. Interfaces* **2012**, *4*, 5483−5491.
(36) Jedaa, A.; Salinas, M.; Jäger, C. M.; Clark, T.; Ebel, A.; Hirsch, A.; Halik, M. Mixed Self-Assembled Monolayer of Molecules with Dipolar and Acceptor Character-Influence on Hysteresis and Threshold Voltage in Organic Thin-Film Transistors. *Appl. Phys. Lett.* **2012**, *100*, 063302.
(37) Wan, A.; Jiang, L.; Sangeeth, C. S. S.; Nijhuis, C. A. Reversible Soft Top-Contacts to Yield Molecular Junctions with Precise and Reproducible Electrical Characteristics. *Adv. Funct. Mater.* **2014**, *24*, 4442−4456.
(38) Halik, M.; Hirsch, A. The Potential of Molecular Self-Assembled Monolayers in Organic Electronic Devices. *Adv. Mater.* **2011**, *23*, 2689−2695.
(39) Sekitani, T.; Zschieschang, U.; Klauk, H.; Someya, T. Flexible Organic Transistors and Circuits with Extreme Bending Stability. *Nat. Mater.* **2010**, *9*, 1015−1022.
(40) Hoque, E.; DeRose, J. A.; Hoffmann, P.; Mathieu, H. J.; Bhushan, B.; Cichomski, M. Phosphonate Self-Assembled Monolayers on Aluminum Surfaces. *J. Chem. Phys.* **2006**, *124*, 174710.
(41) Lee, H. S.; Kim, D. H.; Cho, J. H.; Hwang, M.; Jang, Y.; Cho, K. Effect of the Phase States of Self-Assembled Monolayers on Pentacene Growth and Thin-Film Transistor Characteristics. *J. Am. Chem. Soc.* **2008**, *130*, 10556−10564.
(42) Kim, D. H.; Lee, H. S.; Yang, H.; Yang, L.; Cho, K. Tunable Crystal Nanostructures of Pentacene Thin Films on Gate Dielectrics Possessing Surface-Order Control. *Adv. Funct. Mater.* **2008**, *18*, 1363−1370.
(43) Kim, K. D.; Song, C. K. Low Voltage Pentacene Thin Film Transistors Employing a Self-Grown Metal-Oxide as a Gate Dielectric. *Appl. Phys. Lett.* **2006**, *88*, 233508.
(44) Ma, H.; Acton, O.; Ting, G.; Ka, J. W.; Yip, H. L.; Tucker, N.; Schofield, R.; Jen, A. K. Y. Low-Voltage Organic Thin-Film Transistors with π-σ-Phosphonic Acid Molecular Dielectric Monolayers. *Appl. Phys. Lett.* **2008**, *92*, 113303.
(45) Kobayashi, S.; Nishikawa, T.; Takenobu, T.; Mori, S.; Shimoda, T.; Mitani, T.; Shimotani, H.; Yoshimoto, N.; Ogawa, S.; Iwasa, Y. Control of Carrier Density by Self-Assembled Monolayers in Organic Field-Effect Transistors. *Nat. Mater.* **2004**, *3*, 317−322.
(46) Islam, M. M.; Pola, S.; Tao, Y. T. Effect of Interfacial Structure on the Transistor Properties: Probing the Role of Surface Modification of Gate Dielectrics with Self-Assembled Monolayer Using Organic Single-Crystal Field-Effect Transistors. *ACS Appl. Mater. Interfaces* **2011**, *3*, 2136−2141.
(47) Tseng, C. W.; Chen, Y. L.; Tao, Y. T. Tuning Electric Bistability in Pentacene Film-Based Transistor Embedding Aluminum Nanoparticles. *Org. Electron.* **2012**, *13*, 1436−1442.
(48) Baeg, K. J.; Noh, Y. Y.; Sirringhaus, H.; Kim, D. Y. Controllable Shifts in Threshold Voltage of Top-Gate Polymer Field-Effect Transistors for Applications in Organic Nano Floating Gate Memory. *Adv. Funct. Mater.* **2010**, *20*, 224−230.
(49) Sokolov, A. N.; Cao, Y.; Johnson, O. B.; Bao, Z. Mechanistic Considerations of Bending-Strain Effects within Organic Semiconductors on Polymer Dielectrics. *Adv. Funct. Mater.* **2012**, *22*, 175−183.
(50) Han, S. T.; Zhou, Y.; Roy, V. A. L. Towards the Development of Flexible Non-Volatile Memories. *Adv. Mater.* **2013**, *25*, 5425−5449.
(51) Jedaa, A.; Halik, M. Toward Strain Resistant Flexible Organic Thin Film Transistors. *Appl. Phys. Lett.* **2009**, *95*, 103309.
(52) Olivier, Y.; Lemaur, V.; Brédas, J. L.; Cornil, J. Charge Hopping in Organic Semiconductors: Influence of Molecular Parameters on Macroscopic Mobilities in Model One-Dimensional Stacks. *J. Phys. Chem. A* **2006**, *110*, 6356−6364.
(53) Tessler, N.; Preezant, Y.; Rappaport, N.; Roichman, Y. Charge Transport in Disordered Organic Materials and Its Relevance to Thin-Film Devices: A Tutorial Review. *Adv. Mater.* **2009**, *21*, 2741−2761.

DOI: 10.1021/acsami.5b01625
ACS Appl. Mater. Interfaces 2015, 7, 9767−9775